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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,580	10/01/1998	RICHARD W. ARNOLD	TI-22561	6836

23494 7590 10/18/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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09/164,580

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT	PAPER
	101405

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

This application was returned to examiner by The Board of Patent Appeals and Interferences for locating missing pages of the declaration filed November 15, 2001. Upon contacting Scanning Customer Support, it was found that the document needed to be re-indexed. The documents have been re-indexed and are now viewable in IFW for the board to review.

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

PTO-90C (Rev.04-03)

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD W. ARNOLD,
WELDON BEARDAIN, DANIEL W. PREVEDEL,
DONALD E. RILEY and LESTER L. WILSON

Application 09/164,580

ORDER RETURNING UNDOCKETED APPEAL TO EXAMINER

This application was received electronically at the Board of Patent Appeals and Interferences on September 22, 2005. A review of the application has revealed that the application is not ready for docketing as an appeal. Accordingly, the application is herewith being electronically returned to the examiner. The matters requiring attention prior to docketing are identified below:

A review of the Image File Wrapper (IFW) indicates that on November 15, 2001, a "Supplement to Amendment Under 37 C.F.R. 1.111" was filed which stated:

> [A]ttached hereto are Declarations of the inventors . . . .

However, upon further review, only page 2 of one declaration which was signed by three of the inventors and dated 11/06/01 is appended.

Accordingly, it is

ORDERED that the application is returned to the Examiner:

1) for locating the missing page(s) of the declaration(s) filed November 15, 2001;

2) for having a complete copy of the missing page(s) of the declaration(s) scanned into the IFW;

3) for a written notification to appellants regarding the action taken; and

4) for such further action as may be appropriate.

BOARD OF PATENT APPEALS
AND INTERFERENCES

By: _____

DALE M. SHAW
Program and Resource Administrator
(571) 272-9797

DMS:psb

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265

#10/Declaration
12-12-01
R. Graham

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

RICHARD W. ARNOLD ET AL.

Serial No. 09/164,580 (TI-22561)

Filed: October 1, 1998

For: KNOWN GOOD DIE USING EXISTING PROCESS INFRASTRUCTURE

Art Unit: 2822

Examiner: J. Mitchell

Commissioner for Patents
Washington, D.C. 20231

Sir:

DECLARATION UNDER 37 C. F.R. 1.131

RICHARD W. ARNOLD, LESTER WILSON, DAN PREVEDEL, WELDON BEARDAIN AND DON RILEY declare as follows:

1. THAT they are the applicants in the subject application for Letters Patent;

2. THAT the attached invention disclosure was prepared and signed by them prior to May 19, 1997;

3. THAT they conceived the invention as set forth in the attached invention disclosure and in the subject application for Letters Patent in the United States prior to May 19, 1997 and continually worked on the subject invention up to their reduction to practice as well as up to the filing of the provisional application Serial No. 60/060,800, filed October 3, 1997 as well as subsequent thereto, all in the United States;

4. THAT they reduced the invention to practice as disclosed in the subject application in the United States prior to May 19,1997;

5. THAT all redacted dates in the attached invention disclosure are prior to May 19, 1997.

I declare under penalty of perjury that the above stated facts are true and correct on information and belief.

Richard W. Arnold — Date: 11/6/01

Lester Wilson — Date: 11/06/01

Dan Prevedel — Date

Weldon Beardain — Date: 11/06/01

Don Riley — Date

Copy WJB

DOCKET NO. TI 22561

1. Please suggest a descriptive title for your invention:

Known Good Die using Existing Process Infrastructure (KGD/IE)

2. What is the problem solved by your invention?

The cost of producing Known Good Die is too high for low and medium volume production quantities. The KGD/IE approach enables production of Known Good Die (KGD) at a cost much lower than required by conventional methods.

There are many semiconductor packaging options available to electronics industry Original Equipment Manufacturers. For end products where size and weight are critical, such as wireless telecommunications, an increasingly popular semiconductor package is no package at all: bare semiconductor die offer huge increases in product density and mass, while providing all the functionality of a fully packaged component. A semiconductor product that guarantees the same full temperature and reliability performance in die form as an equivalent packaged form is called a Known Good Die (KGD).

There are many methods for producing Known Good Die. A common method is to insert the die into a temporary package for temperature and reliability testing, then remove the die for sale as KGD. These temporary packages are typically more complicated than a standard plastic or ceramic package, since they allow the die to be easily removed at the end of processing. These packages are also typically much more expensive than a standard package. Custom device packages require an investment into custom test sockets and burnin positions, and the development of a new processing flow through production lines. Typical startup costs for a single KGD product are > $100k.

3. What is your solution to the problem?

Under the KGD/IE approach, Known Good Die are processed in an existing package, so further investment in test and burnin hardware is not required. All hardware required to test and burnin the part has already been purchased, so startup costs for a KGD product are greatly reduced.

A general description of the KGD/IE methodology is described below. The detailed implementation for a specific product is also discussed.

The general KGD/IE system is composed of an IC package, the semiconductor die to be tested, along with layers of compliant material used to position the die inside the package, and an interconnecting layer to provide electrical continuity between the die and the package pins. The system is easily assembled and disassembled, and the costly components can be reused many times.

An exploded view of a generic system is shown in Figure 1. Item 110 is the base of a typical IC package (shown without external leads for clarity), while Item 115 is one of many Package Terminals that connect the die to the package pins. Item 120 is a layer of compliant material used to hold the semiconductor die, Item 130, in position inside the package cavity. Item 135 is one of the bond pads on the surface of the die. Item 140 is the Interconnecting Medium

used to provide continuity between the die and the package. Item 150 is another layer of compliant material used to hold the Interconnecting Medium in place on the surface of the die and package terminals. Item 160 is the package lid. Item 170 is an inverted view of Item 140, showing the Inner Terminals (Item 171), Outer Terminals (Item 172), and Conductive Paths (Item 173) between the two terminals.

The same generic system fully assembled is shown in Figure 2. Item 210 is the IC Package. Items 220 and 250 are the Lower and Upper Compliant Material, respectively. Item 230 is the semiconductor component (Die) to be tested, while Item 240 is the Interconnecting Medium. Item 260 is the Package Lid.

KGD/IE enables low startup costs to produce KGD because the primary element seen during test and burnin, the Package, is the same element used by the standard packaged part. The system is easily disassembled, since most of the major components use any method of permanent adhesion. One notable exception to this is the Lid, which is permanently or semi-permanently attached to the package. During disassembly the lid can be removed and discarded, then the Die, Interconnecting Medium and Compliant Material layers separated. If reasonable care is taken during disassembly, the Package and Interconnecting Medium can be reused several times. This reusability of costly package components further reduces overall KGD processing costs.

Some detailed work has been performed to describe the implementation of KGD/IE for a specific product: the MCM6226B is a 128k x 8 SRAM fabricated by Motorola Semiconductor. Texas Instruments currently assembles this die into a 32 pin ceramic Dual Inline Package (DIP) which was selected as the KGD/IE implementation vehicle.

Figure 3 shows the exploded view of the KGD/IE implementation for the MCM6226B device. Relevant dimensions are included. Item 310 is the header (package) used by the SMJ5C1008JDC device, which is the package used for the standard part that uses the MCM6226B die. Items 311 and 312 show cavity dimensions for the package. Items 315 are the package bond fingers that will match up to the outer bumps (Item 372) of the DTO Membrane (Item 340). Item 320 is the lower layer of compliant material, and Item 350 is the upper layer of compliant material. Item 330 is the die to be tested, MCM6226B. The bond pads (Item 335) of the die match up with the inner bumps (Item 371) of the DTO Membrane. Item 340 is the DTO Membrane in its correct position. Item 360 is the temporary package lid. Item 370 is an inverted representation of item 340, which shows the position of inner and outer bumps, and the conductive traces between them.

Interconnecting Medium

The proposed interconnecting medium in the system is a silicon 'membrane' produced by Diamond Tech One (DTO) of Austin, Texas. The membrane consists of a silicon wafer onto which has been deposited compliant bumps and conductive metallization. When the membrane is assembled into the package, the compliant bumps provide electrical contact between the package bond fingers and the die bond pads through the metallization on the membrane. The bumps are produced by a proprietary process and stand approximately 30um tall. They act like tiny springs, able to be repeatedly compressed to a nominal 50% of their original height while still maintaining electrical continuity.

Since the DTO membrane is silicon, it provides excellent an excellent thermal expansion match to the silicon die. The compliant bumps allow minimal damage to

occur to the bond pads over compression and temperature excursions. Under proper conditions, the bumps can be compressed over 1000 times and still provide excellent electrical continuity, making multiple uses of the membrane very likely.

One disadvantage of the bump process is that overcompression of the bumps results in a severely shortened lifecycle. To compensate for this, the DTO membrane will be designed with standoffs surrounding each bump. The standoffs will be made out of the same material as the compressive portion of the bumps, but will be electrically non-conductive. The standoffs will be patterned onto the substrate to a height that will prevent overcompression of the conductive bumps by excessive pressures.

Figure 4 shows a detail of the proposed DTO membrane. Item 471 is the inner bump, while Item 472 is the outer bump. When assembled, an inner bump rests on each die bond pad, while an outer bump rests on the package bond finger. Item 473 is the conductive trace, most likely aluminum for the initial implementation. Item 474 is the described standoff, which surrounds Item 475, the conductive bump itself. The standoff is shorter than the uncompressed bump, but is deposited to the exact height that will result in optimal compression of the bump under pressures that would normally overcompress the bump. Item 476 is the silicon substrate that supports these structures.

Compliant material

The primary purpose of the compliant material in the KGD/IE system is to position the die and DTO membrane into precise position inside the package. In doing so, it must be able to accommodate slight variations in the thickness of materials in the KGD/IE stackup. The position of die and DTO membrane is critical since the die surface, the DTO membrane surface, and the plane of package bond fingers be nearly coplanar in order for electrical continuity between die bond pads and external package pins to be maintained. These surfaces must be held planar to within the compressive limits of the conductive bumps on the DTO membrane itself. Since the ceramic package and silicon members in the system (die and DTO membrane) have tolerances associated with their specified thickness, it is also necessary the compliant material be able to accommodate variations in component thickness without compromising positioning of the components.

Both layers of compliant material are Gel-Pak, a product of Gel-Pak of Sunnyvale, California (division of Vichem Corp), in its free film form. The material is a polymer of proprietary composition that exhibits tacky properties that make it useful as a die shipping medium. In the KGD/IE system, however, it is used because of its compressive properties. Based on experimental data, it has been determined that the force/compression characteristics of the material make it a good choice for use inside the KGD/IE system. It is expected that standard compositions will be used for this product, although the exact tack level remains to be determined. The dimensions of Gel-Pak material will also be adjusted to provide proper compression characteristics for the system.

In an assembled system, the lower layer of Gel-Pak provides an upward force on the die, raising and aligning it to the plane of the bond finger shelf. The upper layer of Gel-Pak provides a downward force on the DTO Membrane, securely holding and aligning it in place onto the bond fingers and the die bond pads. These forces are generated by compressing the layers during the assembly operation.

System Assembly

The materials shown in Figure 3 are placed in the package cavity by a vision-controlled alignment system. The lid is placed on the stack and forced downward by the assembly equipment. The compliant layers are compressed by this force, providing alignment of the die and interconnecting medium. The lid is attached to the package with a temporary adhesive. Once continuity for the die and package are observed the device is ready to proceed through the test and burn-in flow for integrated circuits.

Variations

It is the intent of this application to describe a method for producing Known Good Die using an existing package and test/burnin infrastructure, independent of the specific implementation of such a system. A wide variety of variations from the presented implementation documented here are possible. Some of these modifications might include the following:

The Interconnecting Medium could be implemented on a different base material, such as ceramic. The conductive bumps could be replaced with other conductive materials, such as a conductive polymer, a polymer embedded with conductive wires, or a miniature coil spring such as a fuzz button. The conductive traces could be any conductive material, and are not limited to a specific pattern or number of connected terminals. A wide variety of compliant materials could be used by varying chemical composition, basic thickness, compressive properties, and temperature performance. A different lid attach method could be implemented by using different epoxies on the seal area or a different lid base material.

In this illustration, there is a one-to-one relationship between the number of Bond Pads and the number of Inner Terminals, and also between the number of Package Terminals and the number of Outer Terminals. However, the method does not preclude the use of more terminals for electrical or structural purposes, as required by a particular implementation. Also note that the thickness of either layer of compliant material can vary depending on the dimensions of the die and package, and due to the material properties of the layer itself. A layer may not even be required for some systems.

The generic stackup illustrated in Figure 1 could also be modified to allow different arrangements or orientations of components. For example, the Interconnecting Medium and Die could be mated together (bond pads touching interconnecting bumps) and the assembly inverted before placing it in the package. In this case, outer bumps would be replaced by bond pads which could be permanently bonded to the package. A variation such as this still performs the function of KGD/IE by allowing temporary testing of a die in an existing package.

4. When was the solution first conceptually or mentally complete?
   Date: __ / ___ / ___

5. What is the first tangible evidence of such completion?
   Date: __ ./ __ / ___

The engineering notebook kept by Richard Arnold (#09170) details an experiment where the lower die and silicon membrane have continuity between the

die and the membrane and package.

6. What is different about your solution, compared with other solutions to the same problem?

This solution utilizes an existing package and existing package infrastructure for test and burn-in. At the present time no other reliable Known Good Die technology makes use of the existing test and burn-in infrastructure. TI can procure the membranes for a fraction of the cost of conventional KGD processing systems, and also avoid the development of custom test hardware and burn-in fixtures required for the production of KGD.

7. What are the advantages of your solution?

Known Good Die using Existing Process Infrastructure is less expensive than conventional test carrier based technology. This cost reduction comes from two sources: the user does not have to set up a special test and burn-in line to manufacture the KGD, and the cost of the KGD/IE hardware is less than a typical temporary die carrier. For example, the cost for a typical temporary carrier system for a low volume line such as a Texas Instruments Military Products Digital Signal Processor is over $550.00, whereas the cost for a KGD/IE approach is approximately $55.00.

8. What TI products, processes, projects or operations currently implement your invention?

Presently we know of no TI product or process that utilizes this invention.

9. What is the date of the first implementation? __ / __ / __ .

With proper TI support we will build a membrane for low pin count memory die 1st quarter .

10. What record exists to prove this date?

Engineering notebooks and other written records document the evolution of this idea. Attached is a dated quotation the for Diamond Tech One membrane.

11. Is there any future implementation planned? (Y/N)
If so, please furnish the TI PART No. or project name.

This approach is ideal for low volume known good die suppliers such as the TI Military Products Division. Any discrete semiconductor product could be processed with this technology, but the first products selected will likely be memory and Digital Signal Processor products.

12. Has the invention been published or disclosed to anyone outside of TI? (Y/N) _Yes_ When? _ If planned when? _____ (catalog, advertising, data book, application note, conference paper, magazine article, TITJ, proposal document.) Was there a nondisclosure agreement (NDA)?

TI has had discussion with Diamond Tech One about this invention and with Gel-Pak about the role of the compliant surface. There are NDAs in place for this technology with both companies.

13. Has a TI product incorporating the invention been

publicly introduced, quoted, sampled or shipped? (Y/N) ____
When?_____ If planned--when?

There has been no product introduced with this process flow.

14. Was the invention conceived or first implemented in the performance of a government contract or subcontract? (Y/N)_____ Contract #:_____

There are no government contracts associated with this invention.

****

THE INVENTION DESCRIBED BY THIS DISCLOSURE IS SUBMITTED PURSUANT TO MY EMPLOYMENT AGREEMENT WITH TEXAS INSTRUMENTS INCORPORATED OR A TI SUBSIDIARY (SPECIFY):

****

Has this disclosure been previously sent to the Patent Department electronically (unsigned)? (Y/N) __YES____

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Witness Date

This invention disclosure with any attachments was read and understood by me on ____/ ____/ ____.

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Date Mail Station

Witness _____ Date _____

This invention disclosure with any attachments was read and understood by me on _____ / _____.

Witness _____ Date _____

This invention disclosure with any attachments was read and understood by me on _____ / _____.

FIGURE 1: GENERIC KGD/IE IMPLEMENTATION EXPLODED VIEW

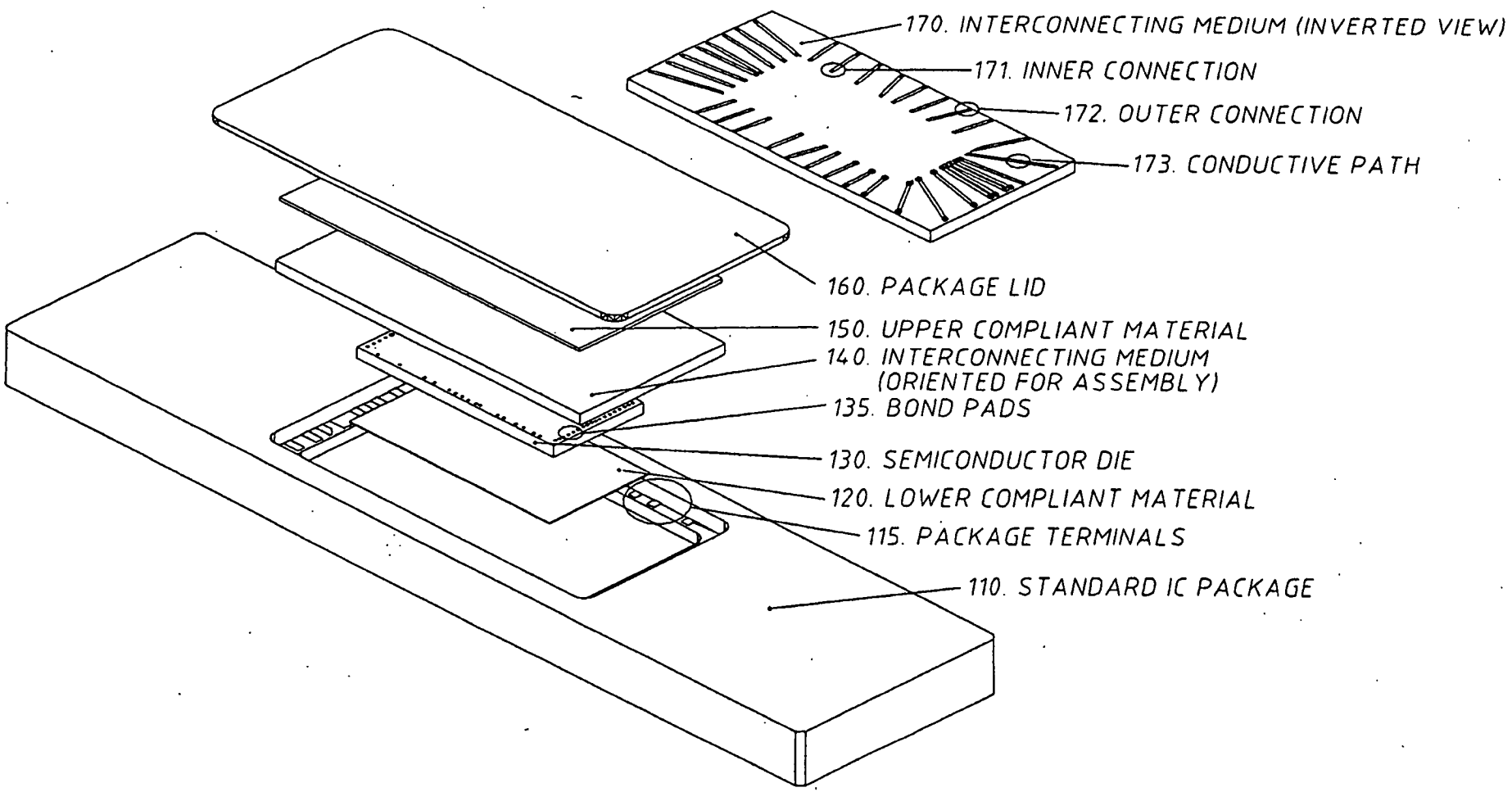

FIGURE 2: GENERIC KGD/IE IMPLEMENTATION, CROSS SECTION OF FULLY ASSEMBLED SYSTEM

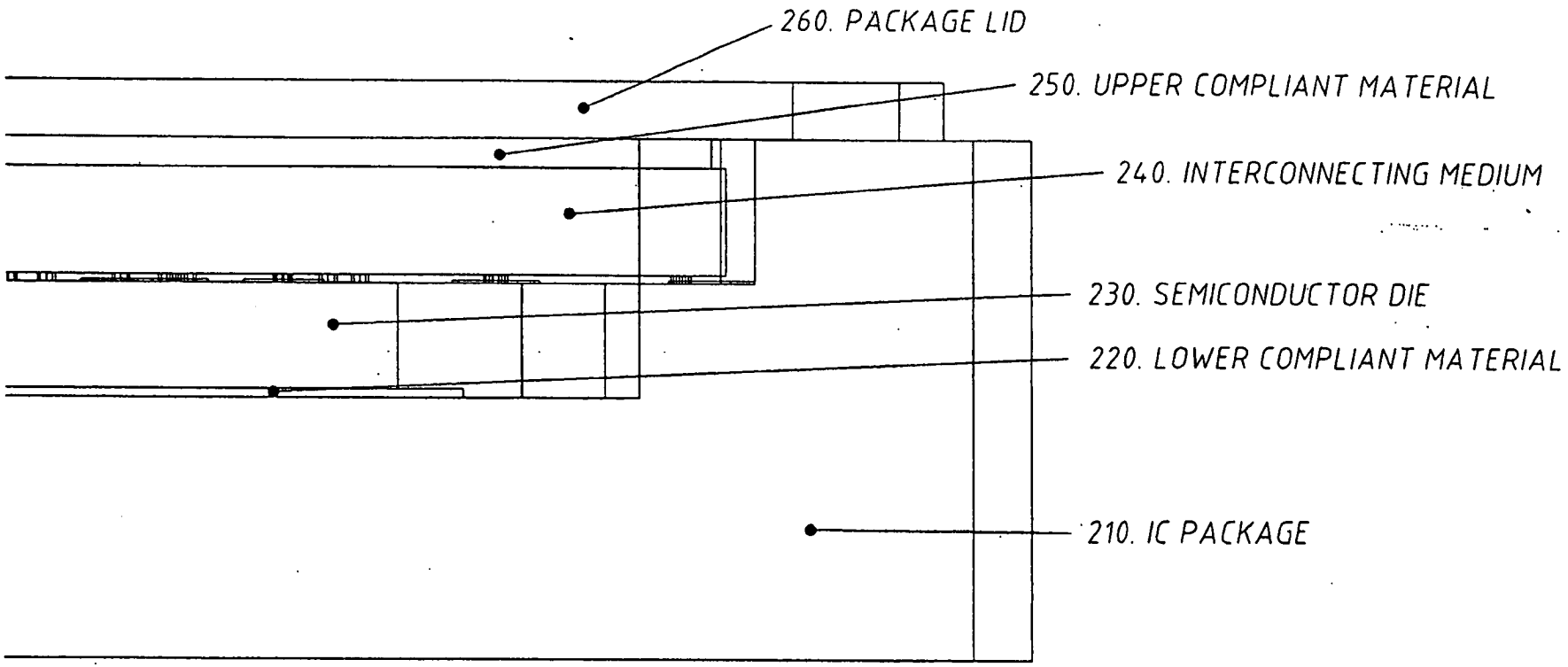

FIGURE 3: KGD/IE IMPLEMENTATION PROPOSAL FOR MCM6226B (1 Mb SRAM)

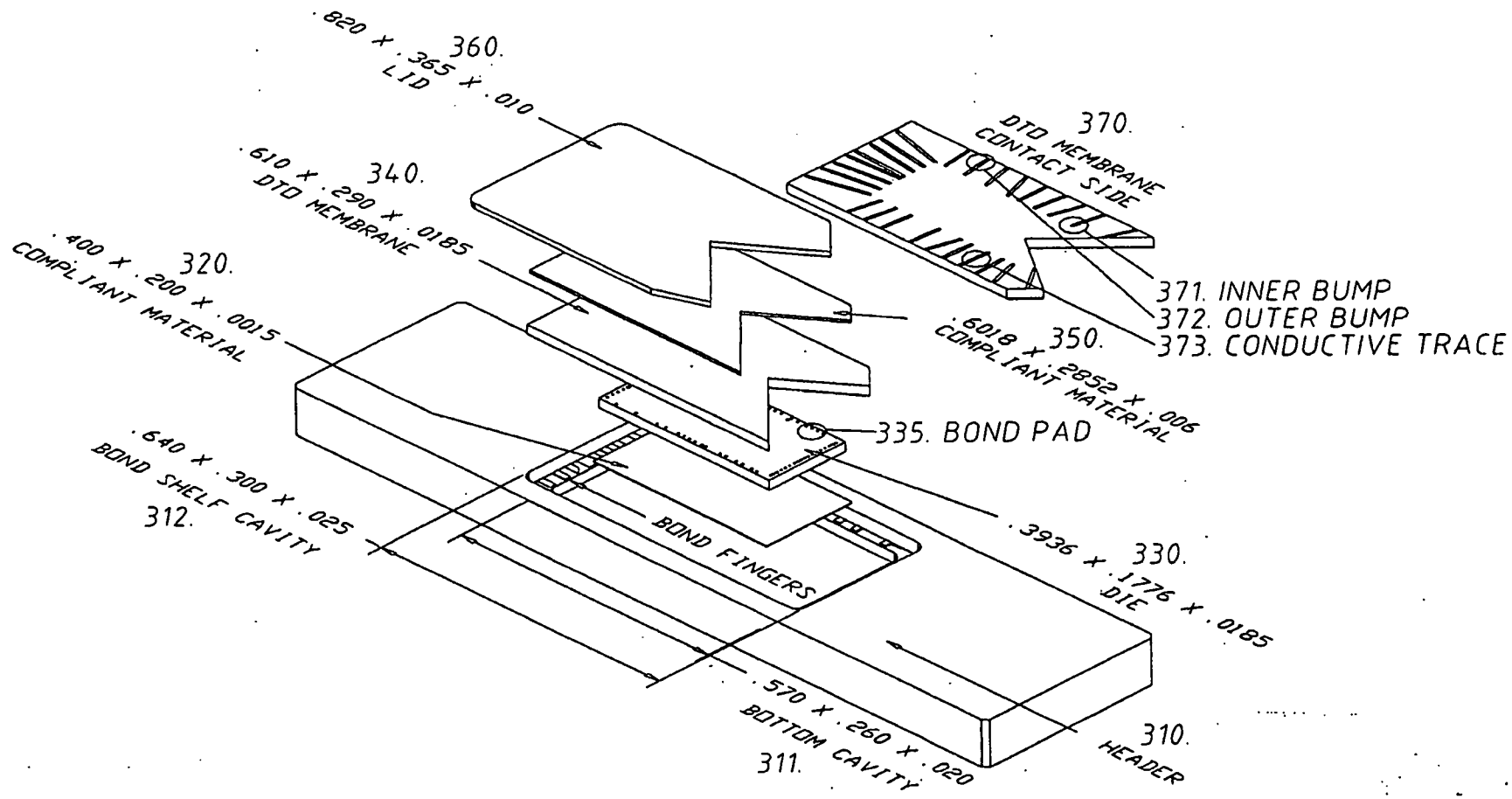

FIGURE 4: DTO MEMBRANE DETAILS